Applicant: Thomas D. FLETCHER

Serial No. 09/893,868

Response to Office Action mailed July 16, 2004

REMARKS

Claims 1-24 are pending in this application. In the last Office Action, claims 1-9, 13 and 14 were rejected under 35 U.S.C. 112, ¶ 2 as being indefinite. Claims 1, 2, 10, 12-18, and 21-24 were rejected under 35 U.S.C. § 102 as being anticipated by Taborn, and claims 16-20 were rejected under 35 U.S.C. § 102 as being anticipated by Winters. Finally, claims 1, 2 and 21-24 were rejected under 35 U.S.C. § 103 as obvious over Winters.

While Applicant does not necessarily agree with the rejections in the last Office Action, this Response cancels claims 2-3 and 18, amends claims 1, 4-6, 10-13, 16, 19, and 21, and adds new claims 25-38 to clarify the claimed invention and to expedite prosecution of this application.

1. Reasons why the rejections under § 112 should be withdrawn

Independent claims 1 and 13 were rejected under § 112, and dependent claims 2-9 and 14 were rejected based on the independent claims.

Applicant submit that the claims as filed were not indefinite. Moreover, as this Response deletes the term "cascaded" from claim 1, Applicant submits that the rejection of claims 1-9 should be withdrawn. As to claim 13, the spelling of the word "complement" has been corrected as suggested in the last Office Action. Finally, Applicant submits that the phrase "Miller coupling" in claim 13 is definite and would be understood by a person of ordinary skill in this art. Applicant notes that, pursuant to MPEP § 2173.02, where an Examiner concludes that a rejection under 35 U.S.C.112, ¶ 2 is appropriate, "an analysis as to why the phrase(s) used in the claim is 'vague and indefinite' should be included in the Office action." See MPEG at page 2100-206. Applicant respectfully submits that the last Office Action did not contain any such analysis, and that the phrase "Miller coupling" is neither vague nor indefinite as understood by a person of skill in the art.

499546_2.DOC - 11 -

Applicant: Thomas D. FLETCHER
Serial No. 09/893,868
Response to Office Action mailed July 16, 2004

2. Reasons why the rejection of claims 1, 4-15 and 21-24 should be withdrawn

Claim 1 has been amended to recite the limitations of claim 2 and claim 3, which was indicated to be allowable in the last Office Action. For at least that reason, Applicant submits that amended claim 1 is allowable.

Claim 10 has been amended to recite the limitations "wherein the first differential domino three-to-two reducer has an input to receive a first clock signal" and "wherein the second differential domino three-to-two reducer has an input to receive a different clock signal" from claim 11, which was indicated to be allowable in the last Office Action. For at least that reason, Applicant submits that amended claim 10 is allowable.

Finally, amended claim 21 recites that the second clock "is delayed from the first clock" as in allowable claim 3. For at least that reason, Applicant submits that amended claim 21 is allowable.

For at least these reasons, claims 1, 10 and 21 are believed to be patentable. Claims 4-9, 11-15 and 22-24 depend from one of claims 1, 10 or 21 and are patentable for at least the same reasons as claims 1, 10 and 21, as well as for additional limitations contained therein.

3. Reasons why the rejection of claims 16, 17, and 19-20 should be withdrawn

Claims 16, 17, and 19-20 were rejected as anticipated by Winters. Applicant respectfully request the withdrawal of these rejections for the following reasons.

As amended, claim 16 recites a differential carry generate gate that has a first evaluation block and a second evaluation block that each have a plurality of transistors, "wherein each of the transistors in the first evaluation block and second evaluation block are part of a transistor stack, and wherein the number of transistors in each of said stacks is the same."

Applicant submit that neither Winters nor any art of record disclose or suggest "wherein each of the transistors in the first evaluation block and second evaluation block are part of a transistor stack, and wherein the number of transistors in each of said stacks is the same." To the contrary, the circuit shown in FIG. 3A of Winters, which the

499546_2.DOC - 12 -

Applicant: Thomas D. FLETCHER

Serial No. 09/893,868

Response to Office Action mailed July 16, 2004 *

last Office Action relies upon in rejecting claim 16, does not meet these limitations. This circuit contains five transistors 25 in a first block and five transistors 26 in a second block. Although each block does contain two stacks with two transistors in each block, each block also contains a single transistor (connected to BH and BL) that is not stacked with any other transistors. Thus, the circuit in FIG. 3A of Winters does not meet the limitation "wherein each of the transistors in the first evaluation block and second evaluation block are part of a transistor stack, and wherein the number of transistors in each of said stacks is the same" of claim 16.

Applicant also notes that there is no evidence of a motivation to modify the prior art references to obtain the claimed invention. *See, e.g., In re Zurko*, 258 F.3d 1379, 1368 (Fed. Cir. 2001) (holding that an Examiner must "point to some concrete evidence in the record" of a motivation to combine or modify the references to support an obviousness rejection).

For at least these reasons, claims 16 is believed to be patentable. Claims 17 and 19-20 depend from claim 16 and are patentable for at least the same reasons as claim 16, as well as for additional limitations contained therein.

4. Reasons why new claims 25-38 are allowable

Applicant submits that new claims 25-38 are allowable. As to claims 33 and 35-38, Applicant notes that these claims are similar to original claims 10 and 12-15. Although original claims 10 and 12-15 were rejected in the last Office Action as anticipated by Taborn, Applicant submits that this rejection should not be applied to new claims 33 and 35-38. In this regard, Applicant notes that independent claim 33 recites a "first differential domino three-to-two reducer" and a "second differential domino three-to-two reducer." See Applicant's specification at page 2, lines 1-21 for a discussion of Domino logic. Applicant submits that Tabor does not disclose a domino three-to-two reducer. In addition, claims 33 also recites that "there are no static stages between the first and second differential domino three-to-two reducers." Applicant submits that neither Taborn, Winters nor any other art of records teaches or suggests a circuit as

499546_2.DOC - 13 -

Applicant: Thomas D. FLETCHER

Serial No. 09/893,868

Response to Office Action mailed July 16, 2004

recited in claim 33 with no static stages between a first differential domino three-to-two reducer and a second differential domino three-to-two reducer.

5. Conclusion

Applicant respectfully requests entry of the above amendments and favorable action in connection with this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. 1.16 or 1.17 to Kenyon & Kenyon Deposit Account No. 11-0600. The Examiner is invited to contact the undersigned at (202) 220-4310 to discuss any matter concerning this application.

Respectfully submitted,

Kenyon & Kenyon

Date: 5ept 24, 2004

Kenneth R. Corsello Registration No. 38,115

(Attorney for Intel Corporation)

KENYON & KENYON 1500 K Street, N.W. Washington, D.C. 20005

Ph.:

(202) 220-4200

Fax.: (202) 220-4201